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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,159	11/18/2003	Junichi Kishida	64272/00001	5285

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EXAMINER	
KO, DANIEL BOKMIN	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,159	KISHIDA ET AL.	
	Examiner	Art Unit	
	Daniel B. Ko	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the application filed on 11/18/2003. Claims 1-25 have been submitted for examination.

Specification

The disclosure is objected to because of the following informalities: missing a brief summary of the drawing for Fig. 6 and wrong description of Fig. 5 on page 4, line 9. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US Patent Application 2003/0172261 A1), hereinafter simply Lee.

Regarding claims 1, 8, 16 and 21, Lee teaches an externally non-addressable memory for outputting an executable code sequence comprising:

a plurality of data storage locations (page 3, paragraph 44, Lee discloses NAND flash memory may stores boot code, operating system and other program or data);

a plurality data lines adapted for outputting data stored in the plurality of data storage locations (page 3, paragraph 46, page 4, paragraph 61, Lee discloses the data read from the NAND flash memory is transferred through the NAND interface);

an internal address register adapted for storing address information associated with a memory location associated with an instruction to be output on the data lines (page 4, paragraph 59; Lee discloses an internal buffer which is equivalent to the register);

means for loading a preselected address into the internal address register upon receipt of run signal representative of a commencement of a preselected code sequence comprised of a plurality of executable instructions stored in the plurality of data storage locations signal (page 4, paragraph 54, paragraph 68); and

counter means for sequentially incrementing the internal address register so that instructions of the code sequence sequentially appear on the data lines until completion thereof (page 5, paragraph 69, Lee discloses the executing a copy loop instruction code in the boot code to read out the code sequence in the NAND memory until finish which is equivalent to sequentially reading the code using counter means).

Regarding claim 2, Lee discloses a memory further comprising means for receiving an externally generated clock signal, wherein the counter means is incremented in accordance with the externally generated clock signal (page 5,

paragraph 79; Lee discloses a size of data loaded to the system memory in the NAND flash memory at one time is determined according to the burst length which is equivalent to externally generated clock signal to sequentially incrementing the register).

Regarding claim 3, Lee discloses a memory further comprising means adapted for receiving the run signal from an associated data device (page 4, paragraph 54; Lee discloses system-initializing signal such as a power up signal, a system reset signal, or a re-reset signal which is equivalent to run signal).

Regarding claims 4, 9, 14, 19, and 23, Lee discloses a memory further comprising means for generating the run signal in accordance with a power on state of an data processing device into which the memory is incorporated (page 4, paragraph 54).

Regarding claims 5 and 24, Lee discloses a memory further comprising means for generating a wait signal corresponding to a duration in which no valid data is available on the data lines (page 4, paragraph 61, Lee discloses a hold or delay in the operation of CPU in response to the system initializing signal which is equivalent to generating a wait signal).

Regarding claims 6, 10, and 18, Lee discloses a memory further comprising an associated, addressable, random access memory into which the code sequence is copied (page 3, paragraph 47).

Regarding claims 7 and 17, Lee discloses a memory further comprising an associated processor device, which processor device is synchronized so as to operate on instructions the code sequence as it is output onto the data lines (page 5, paragraph 79, Lee discloses a size of data loaded to the system memory from the NAND flash memory according to the burst length which is equivalent to device is synchronized).

Regarding claim 11, Lee discloses a bootable NAND flash memory wherein the boot signal generator is comprised of a central processor unit (page 3, paragraph 42, page 4, paragraph 54).

Regarding claims 12 and 15, Lee discloses a bootable NAND flash memory further comprising a means for generating a busy signal representative of a duration in which valid boot data is not available on the data lines (page 4, paragraph 60).

Regarding claims 13 and 25, Lee discloses a data processor comprising:

a central processor unit having CPU address lines and CPU data lines (See Fig. 2, page 3, paragraph 46);

a NAND flash memory having NAND data lines in data communication with the CPU data lines, data associated with such data lines being addressable solely from an address register internal thereto (Fig. 2, paragraph 61, Lee discloses the data read from the NAND flash memory is transferred through the NAND interface);

an externally addressable random access memory having RAM address lines in data communication with the CPU address lines and RAM data lines in data communication with the CPU data lines and with the NAND data lines (Fig. 4, page 4, paragraph 64);

a boot code sequence disposed in a series of memory locations of the NAND flash memory (page 4, paragraph 54);

means adapted to generate a boot commencement signal so as to preload the address register with a preselected address associated with the boot code (page 4, paragraph 54);

means for sequentially outputting instructions of the boot code disposed in the NAND flash memory to the NAND data lines from which the boot code is copied via the RAM data lines into memory locations of the random access memory (page 3, paragraph 52); and

means for commencing operation of the central processor unit from boot code disposed in the random access memory after transfer thereof from the NAND memory (page 3, paragraph 49).

Regarding claims 20, Lee discloses a method further comprising the step of transferring instructions from a secondary memory device upon completion of the code sequence (page 3, paragraph 49).

Regarding claims 22, Lee discloses a memory wherein the plurality of data storage locations include nonvolatile memory cells (page 3, paragraph 44, Lee discloses a NAND flash memory which is a type of nonvolatile memory).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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AU 2189

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER